AMENDMENT TO THE CLAIMS

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

1. (previously presented) A method for function testing an emulated logic circuit, comprising the steps of:

- loading a model of the logic circuit into a hardware emulator in a hardware description language,
- putting the emulated logic circuit into an operating mode in which some or all of the flip-flops it contains, in particular with additional logic elements as interfacing circuitry, are functionally chained into one or more shift registers, and
- comparing structural arrangement of the logic circuit in the hardware emulator with structural arrangement of the model of the logic circuit at least partially with the assistance of the operating mode.

2. (previously presented) The method according to claim 1, further comprising the steps of:

- applying a test pattern to inputs of the emulator, the emulator inputs representing inputs of shift registers, and shifting the pattern into the shift registers by means of suitable pulsing,
- setting the emulated logic circuit to a standard operating mode whereby one or more pulsing cycles ensue and the circuit then re-sets to an original operating mode,
- shifting the ensuing result pattern by means of suitable pulsing to emulator outputs which simultaneously represent outputs of the shift registers, and carrying out a check to determine whether the pattern matches an expected value, and
- using a check result to compare the structural arrangement of the logic circuit in the hardware emulator with the structural arrangement of the model of the logic circuit.

3. (previously presented) The method according to claim 1, further comprising the steps of:

- applying a test pattern to an emulator input, the test pattern representing an input of a shift register, and shifting the test pattern through the shift register by means of suitable pulsing,
- checking an emulator output, which simultaneously represents the output of this shift register, for the appearance of the test pattern or of an inverted test pattern,
- determining a number of flip-flops in the shift register from a number of pulsing sequences required for shifting through, and
- using results of the step of determining in a comparison of the structural arrangement of the logic circuit in the hardware emulator with the structural arrangement of the model of the logic circuit.

4. (previously presented) The method according to claim 3, further comprising the steps of connecting an output of a shift register to an input of a next adjacent shift register, and chaining all shift registers into a single shift register by means of recursion.

5. (previously presented) The method according to claim 1, further comprising the steps of:

- in the event that the structural arrangement of the logic circuit in the hardware emulator does not match the structural arrangement of the model, carrying out an analysis to determine sources of such faults, and
- automatically reloading the model of the logic circuit into the hardware emulator with these sources of faults deactivated.

6. (previously presented) A device for testing an emulated logic circuit, comprising:

- a hardware emulator for emulating a logic circuit present in the form of a model,
- a test pattern generator module arranged to apply a test pattern to an input of the hardware emulator,
- a pulse generator arranged to inject a pulse into the hardware emulator,
- a test pattern checking module arranged to check whether a bit pattern being applied to an output of the hardware emulator matches an expected value,

- a module for comparing a structural arrangement of the logic circuit in the hardware emulator with a structural arrangement of a model of the logic circuit at least partially with the assistance of an operating mode of the logic circuit in which some or all of the flip-flops it contains, in particular with additional logic elements as interfacing circuitry, are functionally chained into one or more shift registers.

7. (previously presented) The device according to claim 6, further comprising a module for determining the number of flip-flops in the shift register from a number of pulse sequences needed to shift a test pattern through the register and a module for briefly changing over the logic circuit to a standard operating mode for one pulse cycle or several pulse cycles while a test pattern is being shifted through the register.

8. (previously presented) The device according to claim 6, further comprising a module for chaining all the shift register into a single shift register by means of recursively connecting the output of one shift register to the input of a next adjacent shift register.

9. (previously presented) The device according to claim 6 further comprising:
- a module for analyzing the sources of faults leading to a lack of matching between the structural arrangement of the logic circuit in the hardware emulator and the structural arrangement of the model, and
- a module for automatically loading the model of the logic circuit into the hardware emulator with the sources of faults deactivated.

10. (previously presented) The device according to claim 6, further comprising a module for determining the number of flip-flops in the shift register from a number of pulse sequences needed to shift a test pattern through the register or a module for briefly changing over the logic circuit to a standard operating mode for one pulse cycle or several pulse cycles while a test pattern is being shifted through the register.